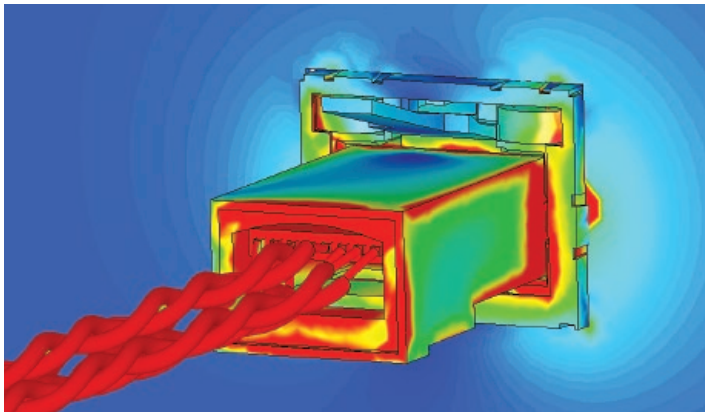
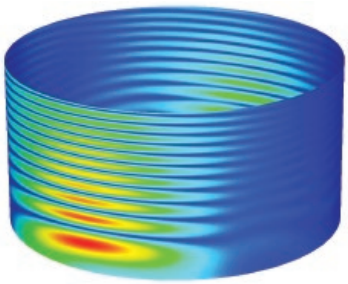
CST STUDIO SUITE

EMC Simulation for Electronic Products

By law, products must comply with international EMC standards which have been developed to regulate electromagnetic emissions and the susceptibility of electrical and electronic systems. Striking a balance between EMC and competing design requirements poses major challenges to engineers. By including EMC compliant design at an early stage, additional costly development iterations can be avoided later on down the line. Simulation allows problems to be identified and corrected early in the design process, before the first prototype is built.



Current leakage around an Ethernet connector

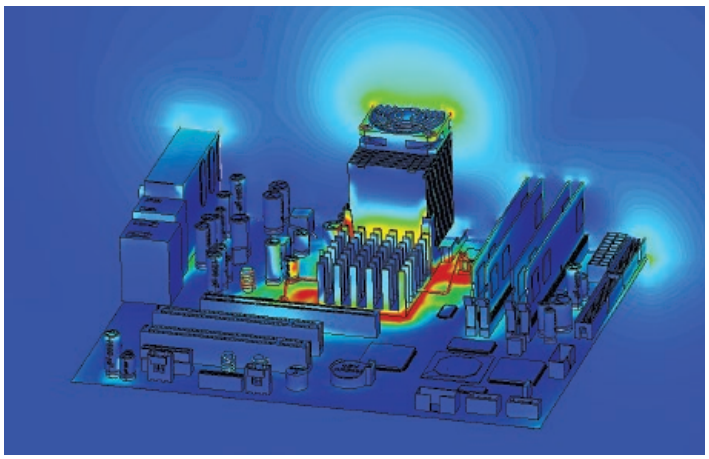


Cylinder scan of radiated fields from an enclosure at 3m distance

Emissions

The geometry of a design and the placement of components both have major effects on the level of radiated and conducted emissions from a device. For example, the layout of reference conductors in an electronic system can have a significant impact on their EMC performance, and so careful PCB design is needed to minimize the risk of EMC issues.

However, increasing PCB complexity means that potential problems can no longer be identified by manual inspection alone. CST BOARDCHECK™ analyzes complete printed circuit boards quickly, checking the layout against EMC and SI design rules. Once potential problems have been identified, the design can be modeled in a 3D full-wave simulator, CST MICROWAVE STUDIO®, in order to perform a more thorough analysis. The 3D full-wave simulator can accurately calculate radiated EM fields from the device, which are often a problem in high-speed electronics, as well as couplings on the device that can lead to conducted emissions problems. Low frequency EMC from power electronics can also be analyzed through integration with the circuit simulator in CST DESIGN STUDIO™.



Radiation from an edge of a multilayer PCB

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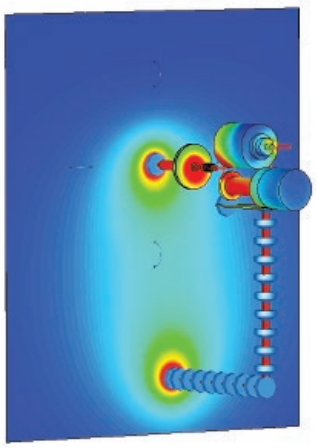
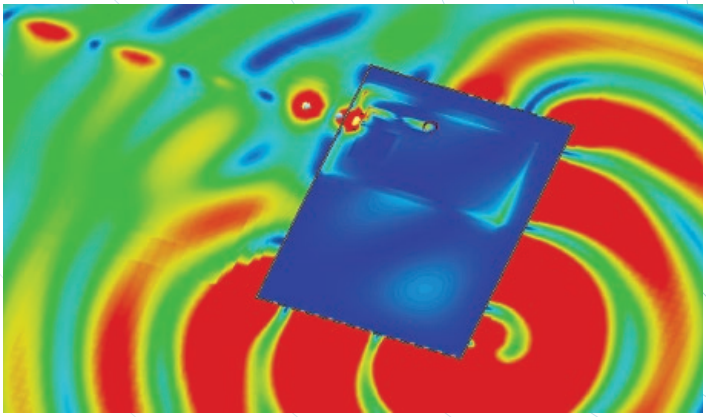
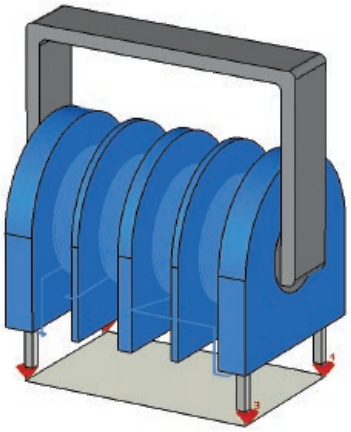


Surface current distribution of a highly detailed model of an ESD Generator



Coupling from an external wifi antenna onto the shield of a cable. From the cable shield, the field couples through a connector to an inner PCB.



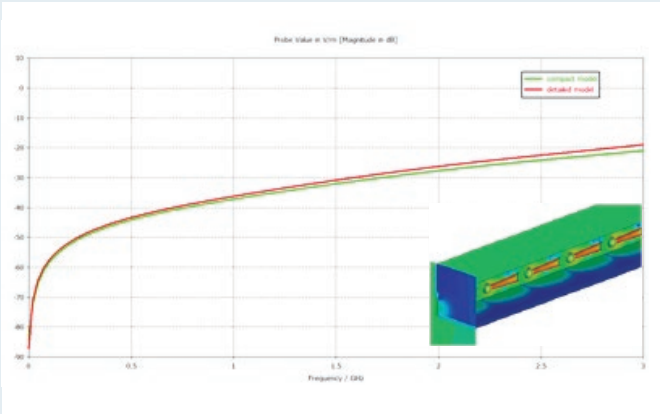
Detailed model of a common mode choke

Susceptibility

As well as establishing emissions limits, EMC regulations also specify the maximum allowed susceptibility of electronic devices. Products have to operate safely in their environment, and therefore must be immune from external influences like irradiation or conducted coupling which can affect the performance of a device or cause it to fail. This type of event is difficult to trace through testing and measurements, and the coupling paths are often unclear. A simulation in CST MICROWAVE STUDIO can visualize fields and currents of an ESD event inside the device, allowing the engineer to identify critical areas and apply countermeasures. Another typical susceptibility concern is the coupling of EM energy through cables connected to the device. Cable entry susceptibility can be easily analyzed using CST CABLE STUDIO®, a specialized simulation tool for cables. The sophisticated bi-directional coupling of the cable solver to the 3D full-wave simulator makes calculations quick and accurate.

Components

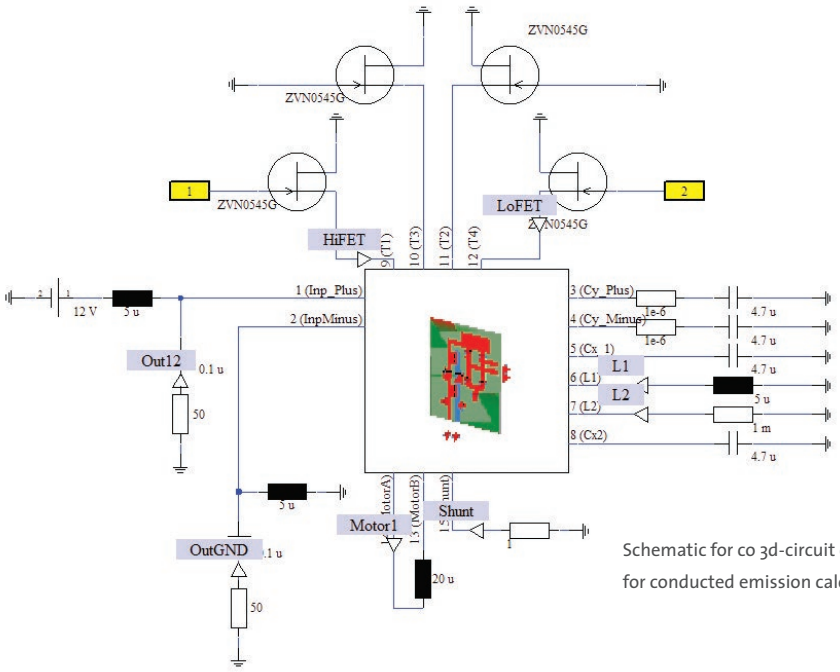
A typical modern electronic device consists of numerous components, from chokes and filters to cables and enclosures. The assortment of solvers inside CST STUDIO SUITE® means that the best numerical method for a structure is always at hand. Highly resonant filters can be modeled efficiently with 3D frequency domain methods, while 3D simulation results can be coupled to a circuit simulator to test the effects of protective devices like suppression diodes. With simulation, engineers can optimize their grounding strategies, design shields to protect the device, and quickly simulate the fine seams, slots and vents found in the enclosures of electronic products using compact models.



Compact Models

The CST MWS TLM solver features “compact modeling” technology. In EMC/EMI applications, objects with relatively small dimensions, such as slots/seams, vents, wires, shielded cables or even special materials have a big impact on the performance of the system. Compact modeling enables these critical features to be represented by equivalent and efficient models to significantly speed up the simulation.

Comaprision of full 3D and compact model results for a complex seam geometry.



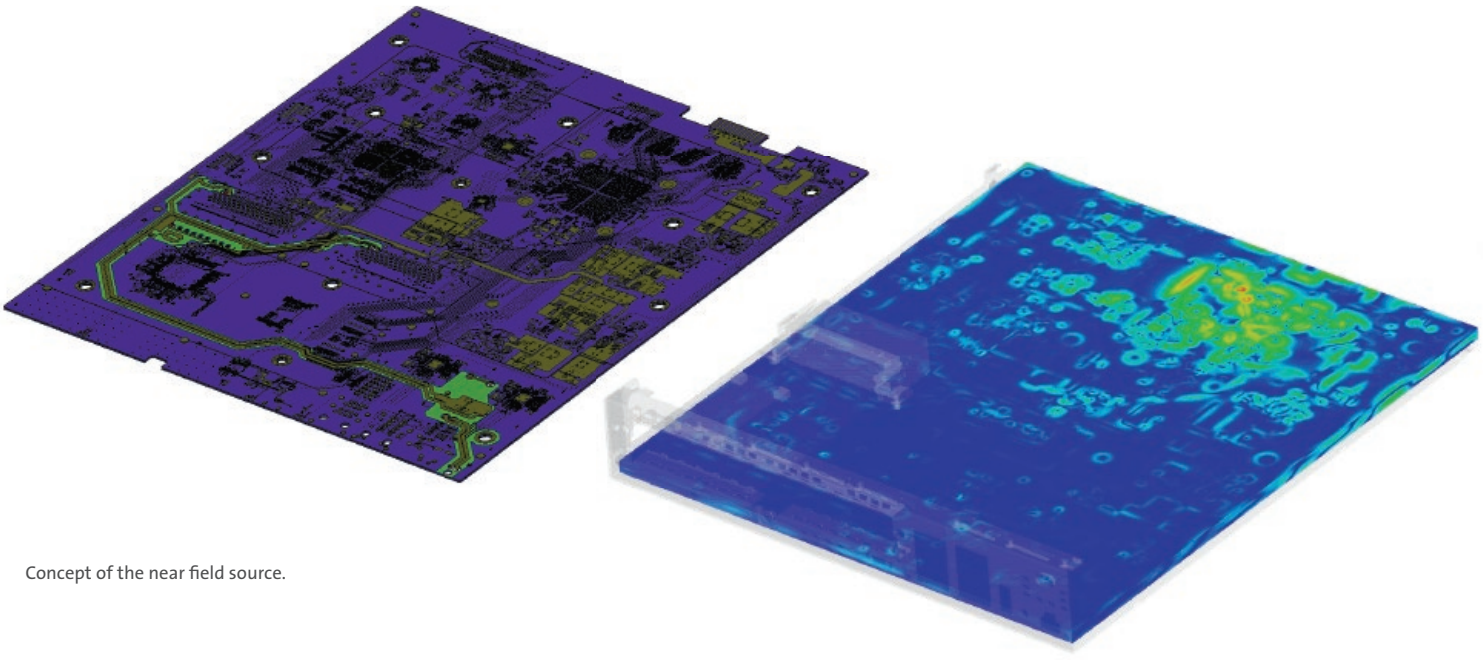
Schematic for co 3d-circuit co-simulation for conducted emission calculation.

System Level Simulations

The tight integration of 3D and system simulation enhances the modeling capabilities of CST STUDIO SUITE, and can substantially speed up the complete analysis of a system. Due to advanced co-simulation capabilities such as CST's unique true transient simulation, fields can be visualized even when the simulation includes circuit components like IBIS, SPICE or Touchstone. Furthermore, the general simulation workflow management approach known as System Assembly Modeling (SAM) gives great flexibility when setting up complex simulation projects. With SAM, field sources can be used to create hybrid simulations, and with parameterization across different projects, components can be combined into assemblies and postprocessing methods can be nested.

True Transient Co-Simulation

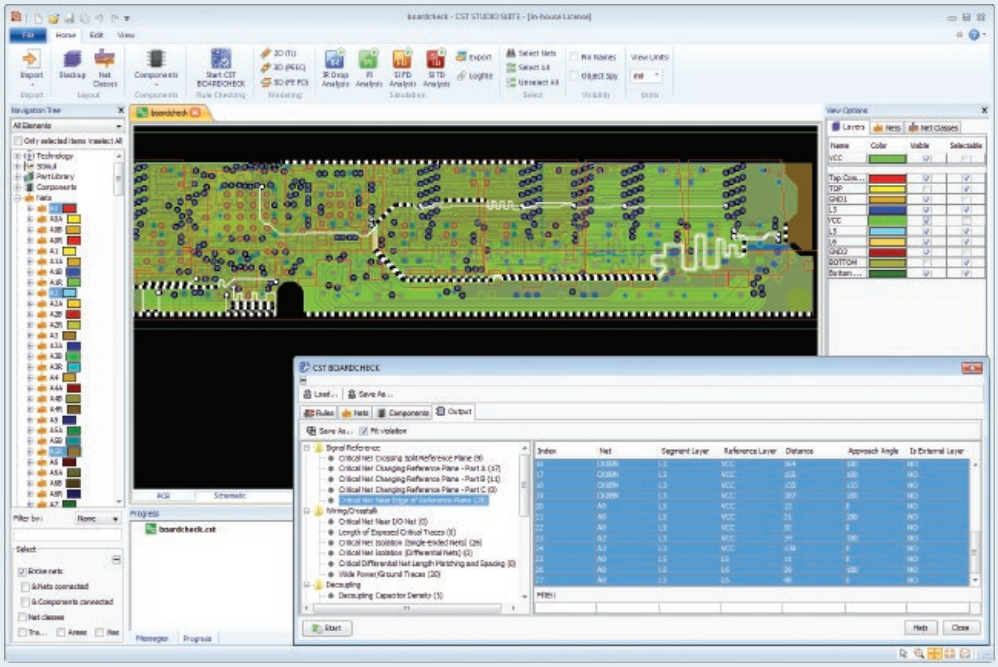
True transient co-simulation is a feature unique to CST, compatible with 3D transient solvers. In the true transient co simulation, circuit elements can be attached to a 3D model and simulated together, with time stepping performed at the circuit and 3D level simultaneously. This means that non-linear circuit elements can be included in the 3D simulation, allowing fields and currents to be visualized in 3D even when these elements are present. True transient methods are very powerful for certain application classes, such as ESD simulations with protective elements or the bi-directional cable simulation.



Concept of the near field source.

Features

- Imports for 3D and EDA CAD models
- Rule-based boardchecking
- Full-wave 3D solvers in the time and frequency domain
- Specialized cable module with arbitrary cable complexity
- Coupling to circuit simulation in time and frequency domain
- Support for IBIS, SPICE and Touchstone
- Outputs: near and farfield, cylinder scan, S/Z/Y parameters, RLC extraction, and voltages & currents in both time & frequency domain
- High performance computing (GPU, MPI)



A violation reported by CST BOARDCHECK

CST BOARDCHECK

The EMC performance of a printed circuit board is mostly based on the placement of components and nets. Manually checking all the layers of today's high speed circuit boards is too time-consuming and prone to human error. CST BOARDCHECK reduces the human error involved in the rule checking processes. CST BOARDCHECK rigorously analyzes complete PCBs against a list of selected EMC or SI design rules. After the rule checking is completed, all EMC rule violations found in the design can be easily located.