# eASIC REDUCES MULTI-LEVEL PACKAGE DESIGN TIMES WITH CST MICROWAVE STUDIO

## THE IDEA: QUICK, CUSTOMIZABLE SEMICONDUCTOR DEVICE DESIGNS

eASIC is a fabless semiconductor company specializing in Single Mask Adaptable ASIC™ (application-specific integrated circuits). They produce custom integrated circuits for a wide range of applications, designed with the specific needs of the customers in mind. Supporting customers effectively, especially during the development stage of a new product, requires a rapid, cost-effective design and manufacturing process.

When designing a chip for a high-speed application, it's not only the behavior of the IC itself that counts. The whole channel, including the package and the printed circuit board (PCB), affects the performance. By taking the PCB layout into account during the design stage, eASIC can improve the performance of the device and reduce the risk of problems emerging once installed.

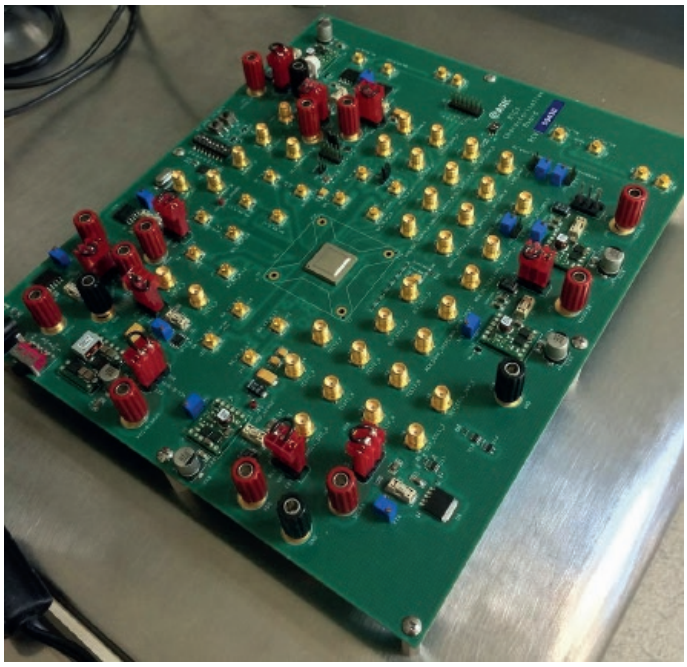

**Figure 1** An eASIC board using a latest device family

## THE CHALLENGE: SIMULATING THE COMPLEX PACKAGE-PCB INTERFACE

Electromagnetic simulation can allow the engineer to investigate the characteristics of a design before committing to manufacturing. Because PCBs are both large and complex while packages are small and intricate, modeling the entire system in one go is computationally intensive, requires long simulation times and heavy memory consumption. For this reason, eASIC decided to split the simulation, and model the package and PCB separately.

For this, eASIC chose CST MICROWAVE STUDIO® (CST MWS), a full-wave 3D simulation tool. CST MWS includes System Assembly and Modeling (SAM), which allows simulations to be linked and cascaded, so that the system can be considered as the sum of its parts. The existing combined package/PCB models were decomposed to separate the two parts, and were linked using ports with a reference plane at the interface (Figure 2).

**About eASIC**

eASIC is a fabless semiconductor company offering breakthrough Single Mask Adaptable ASIC devices aimed at dramatically reducing the overall cost and time-to-production of customized semiconductor devices. Low-cost, high-performance and fast-turn ASIC and System-on-Chip designs are enabled through patented technology utilizing Via-layer customizable routing. This innovative fabric allows eASIC to offer a new generation of ASICs with significantly lower up-front costs than traditional ASICs.

Privately held eASIC Corporation is headquartered in Santa Clara, California. Investors include Khosla Ventures, Kleiner Perkins Caufield and Byers (KPCB), Crescendo Ventures, Seagate Technology (NASDAQ:STX) and Evergreen Partners.

For more information on eASIC please visit **www.easic.com**.

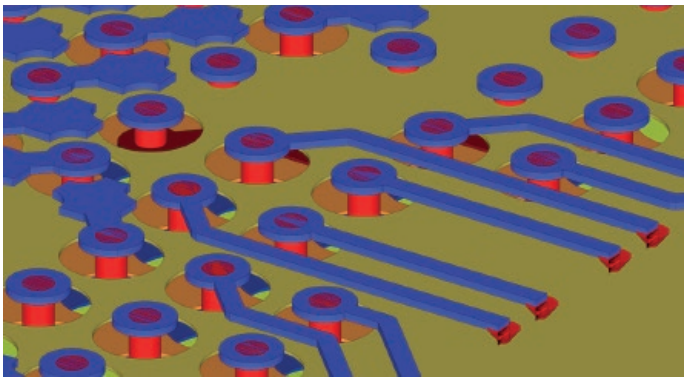

**Figure 2** The package pins and the interface between a package and a PCB, marked with red ports

## THE RESULT: ACCURATE FULL-WAVE SIMULATIONS IN HALF THE TIME

Compared to the simulation of the full model, the co-simulation using SAM was significantly faster and less computationally demanding. The co-simulation results matched both the full simulation results and actual measurements closely (Figure 3). Simulation was also able to accurately replicate widely-used laboratory measures such as time-domain reflectometry (TDR). By using CST MWS and partitioning the model, eASIC was able to achieve up to five-fold speed-up in its multi-level PCB and package simulations, when compared with simulation using the full model. This gave eASIC a significant speed advantage and helped them to shorten the design process.

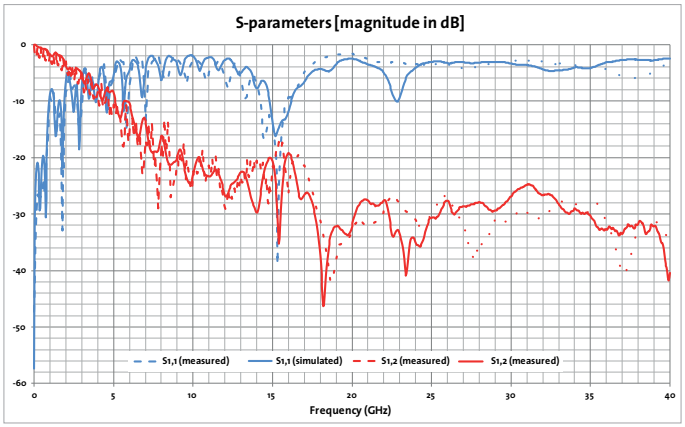


**Figure 3** S-parameters

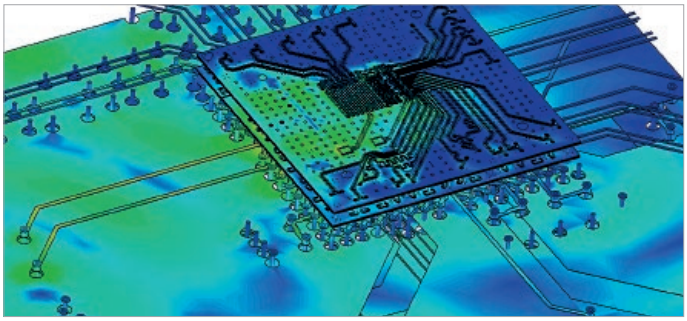

**Figure 4** Simulated surface current distribution across a PCB and package

*"Package-PCB co-design through a segmentation approach in CST MWS, enabled us to leverage 3D EM simulation strength in an accurate analysis of the interconnect with model fitting on a cost-effective server machine in a reasonable run time. This is an amazing way to make full 3D simulation in complex designs a reality!"*

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